AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Currently Amended)* Data processing apparatus comprising:

(i) a main processor responsive to program instructions to perform data processing operations; and

(ii) a coprocessor coupled to said main processor and responsive to a coprocessor load instruction on said main processor to load one or more loaded data words into said coprocessor and perform at least one coprocessor processing operation specified by said coprocessor load instruction using said one or more loaded data words to provide operand data to generate at least one result data word;

(iii) wherein in response to said coprocessor load instruction, said coprocessor is configured to load a variable number of loaded data words in dependence upon whether a start address of said operand data within said one or more loaded data words is aligned with a word boundary; and

(iv) wherein said coprocessor includes an alignment register for storing a value specifying alignment between said operand data and said one or more loaded data words.

2. *(Previously Presented)* Data processing apparatus as claimed in claim 1, wherein said coprocessor includes a coprocessor memory for storing one or more locally

stored data words used as operands in said at least one coprocessor processing operation in combination with said one or more loaded data words.

3. *(Previously Presented)* Data processing apparatus as claimed in claim 1, comprising a memory coupled to said main processor and wherein said main processor is configured to retrieve said one or more loaded data words from said memory to said coprocessor via said main processor without being stored within registers within said main processor.

4. *(Original)* Data processing apparatus as claimed in claim 1, wherein said main processor includes a register operable to store an address value pointing to said one or more data words.

5. *(Original)* Data processing apparatus as claimed in claim 1, wherein said at least one coprocessor processing operation includes calculating a sum of absolute differences between a plurality of byte values.

6. *(Previously Presented)* Data processing apparatus as claimed in claim 5, wherein said coprocessor is arranged to calculate said sum of absolute differences as a sum of absolute differences between a plurality of byte values within said one or more

loaded data words and corresponding ones of a plurality of byte values within said one or more locally stored data words.

7. *(Previously Presented)* Data processing apparatus as claimed in claim 6, wherein said coprocessor includes an accumulate register for accumulating said sum of absolute differences.

8. *(Cancelled)*

9. *(Original)* Data processing apparatus as claimed in claim 4, wherein said coprocessor load instruction includes an offset value to be added to said address value upon execution.

10. *(Original)* Data processing apparatus as claimed in claim 1, wherein said at least one coprocessor processing operation calculates a sum of absolute differences as part of block pixel value matching.

11. *(Currently Amended)* A method of processing data comprising the steps of:

(i) in response to program instructions, performing data processing operations in a main processor; and

(ii) in response to a coprocessor load instruction on said main processor, loading one or more loaded data words into a coprocessor coupled to said main processor and performing at least one coprocessor processing operation specified by said coprocessor load instruction using said one or more loaded data words to provide operand data to generate at least one result data word;

(iii) wherein in response to said coprocessor load instruction, a variable number of loaded data words are loaded into said coprocessor in dependence upon a value stored in an alignment register within said coprocessor, said value indicating whether a start address of said operand data within said one or more loaded data words is aligned with a word boundary.

12. *(Currently Amended)* A computer program product for controlling a computer to perform the steps of:

(i) in response to program instructions, performing data processing operations in a main processor; and

(ii) in response to a coprocessor load instruction on said main processor, loading one or more loaded data words into a coprocessor coupled to said main processor and performing at least one coprocessor processing operation specified by said coprocessor load instruction using said one or more loaded data words to provide operand data to generate at least one result data word;

(iii) wherein in response to said coprocessor load instruction, a variable number of loaded data words are loaded into said coprocessor in dependence upon a value stored in an alignment register within said coprocessor, said value indicating whether a start address of said operand data within said one or more loaded data words is aligned with a word boundary.